

Abstract of the Disclosure

In a method for fabricating a metal oxide semiconductor (MOS) transistor, which can reduce the junction capacitance without a degradation of characteristics in a transistor even in gate line narrowing, the method comprising the steps of: forming a buffer oxide layer on a semiconductor substrate having an isolation layer; successively conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer; removing the buffer oxide layer; forming a sacrificial layer of the semiconductor substrate; patterning the sacrificial layer to form a trench defining a gate electrode forming region; successively conducting ion implantations for threshold voltage adjustment and punch stop formation on the semiconductor substrate area exposed by the trench; forming a gate oxide layer on the surface of the substrate under the bottom face of the trench; forming a polysilicon layer on the sacrificial layer so as to completely bury the trench; polishing the polysilicon layer until the surface of the sacrificial layer is exposed, so as to form a gate electrode; removing the sacrificial layer; forming an LDD region in the surface of the substrate at both side portions of the gate electrode; forming

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spacers on both side walls of the gate electrode; and forming the source/drain regions in the surface of the substrate at both side portions of the gate electrode including the spacers.